WHAT IS CLAIMED IS:

1. A leakage current control device, comprising:

a circuit having one or more functions in a data path where the functions are executed in a sequence, each of the functions having power reduction logic to selectively energize each respective function; and

a leakage control circuit, which interacts with the power reduction logic, so that the functions are energized or deenergized in a control sequence such the functions where the data is resident are energized and at least one of the other functions is not energized.

2. The device as recited in claim 1, wherein the circuit includes combinational logic.

3. The device as recited in claim 1, wherein the circuit includes a pipeline and the functions include combinational logic in a pipeline stage.

4. The device as recited in claim 1, wherein the circuit includes a pipeline and the functions include sequential logic in a pipeline stage.

5. The device as recited in claim 1, wherein the circuit includes a pipeline and tile functions are included in one or more stages of the pipeline.

6. The device as recited in claim 1, wherein the power reduction logic is divided into individually enabled portions, each portion being enabled in accordance with the control sequence.

7. The device as recited in claim 1, wherein the power reduction logic is divided into individually enabled portions, each portion having a threshold voltage adjusted for transistors within each respective portion in accordance with the control sequence.

8. The device as recited in claim 7, wherein the threshold voltage for transistors is adjusted within each respective portion by controlling body biasing of the transistors.

9. The device as recited in claim 1, wherein the power reduction logic is energized in accordance with a pulse wave.

10. The device as recited in claim 9, wherein the

pulse wave is shorter than a clock cycle time.

11. The device as recited in claim 1, wherein the power reduction logic is energized in accordance with a front edge of a pulse wave and at least partially deenergized in accordance with a back edge of the pulse wave.

12. The device as recited in claim 1, wherein at the power reduction logic is divided into individually enabled portions such that only a subset of the portions are energized at a time.

13. The device as recited in claim 12, wherein a pulse wave controls the individually enabled portions of the power reduction logic by adjusting transistor body bias.

14. The device as recited in claim 1, wherein the leakage control circuit selectively employs retentive and non-retentive means to reduce current leakage.

15. The device as recited in claim 14, wherein the retentive means includes body biasing of transistors.

16. The device as recited in claim 14, wherein the retentive means includes partial supply voltage and/or ground gating.

17. The device as recited in claim 14, wherein the nonretentive means includes supply voltage and/or ground gating.

18. The device as recited in claim 1, wherein the leakage control circuit controls power in the functions based on look-behind feedback from upstream functions in the data path.

19. The device as recited in claim 1, wherein the leakage control circuit controls power in the functions based on look-ahead feedback from downstream functions in the data path.

20. The device as recited in claim 1, wherein the device is employed in a system and performs at a subunit level, wherein the leakage control circuit selectively controls power at the subunit level in conjunction with system level power control to reduce current leakage and reduce power consumption.

21. The device as recited in claim 20, wherein individual components of the subunit are controlled at a component level by the leakage control circuit to selectively control power.

22. A leakage current control device comprising:

a pipeline having one or more stages, each stage including sequential logic and combinational logic, and being executed in a sequence, each of the stages having power reduction logic to selectively energize the respective stage; and

a leakage control circuit which energizes, in a control sequence, the stages so that data progresses along the pipeline path to be resident at each stage in the sequence when the stage is energized and at least one of the other pipeline stages is not energized.

23. The device, as recited in claim 22, further comprising:

one or more look behind inputs to the leakage control circuit, each of the look behind inputs monitoring whether there is data in a prior stage of the pipeline; and

a leakage control process that de-energizes one or more current stages if: there is no data in the current stage and each of the look behind input indicates there is no data in one or more of the prior stages.

24. The device as recited in claim 22, further comprising:

one or more look ahead inputs to the leakage control circuit, each of the look ahead inputs monitoring whether there is a data hold condition in a subsequent stage of the pipeline; and

a leakage control process that at least partially de-energizes one or more current stages if: there is valid data in a current stage, the current stage is in a data hold condition, and all of the look ahead inputs indicate there is a data hold condition.

25. The device as recited in claim 24, wherein a stage is partially de-energized if the stage includes valid data and is in a data hold condition.

26. The device as recited in claim 22, the power reduction logic is divided into individually enabled

portions, each portion being enabled in accordance with a control sequence.

27. The device as recited in claim 22, wherein the power reduction logic is divided into individually enabled portions, each portion having a threshold voltage adjusted for transistors within each respective portion in accordance with a control sequence.

28. The device as recited in claim 27, wherein the threshold voltage for transistors is adjusted within each respective portion by controlling body biasing of the transistors.

29. The device as recited in claim 22, wherein the leakage control circuit selectively employs retentive and non-retentive means to reduce current leakage.

30. The device as recited in claim 29, wherein the retentive means includes body biasing of transistors.

31. The device as recited in claim 29, wherein the retentive means includes partial supply voltage and/or ground gating.

32. The device as recited in claim 29, wherein the nonretentive means includes supply voltage and/or ground gating.

33. The device as recited in claim 22, wherein the device is employed in a system and performs at a subunit level, wherein the leakage control circuit selectively controls power at the subunit level in conjunction with system level power control to reduce current leakage and reduce power consumption.

34. The device as recited in claim 33, wherein individual components of the subunit are controlled at a component level by the leakage control circuit to selectively control power.

35. The device as recited in claim 22, wherein the power reduction logic is energized in accordance with a pulse wave.

36. The device as recited in claim 35, wherein the pulse wave is shorter than a clock cycle time.

37. The device as recited in claim 22, wherein the power reduction logic is energized in accordance with a

front edge of a pulse wave and at least partially deenergized in accordance with a back edge of the pulse wave.

38. The device as recited in claim 22, wherein the power reduction logic is divided into individually enabled portions such that only a subset of the portions are energized at a time.

39. The device as recited in claim 39, wherein a pulse wave controls the individually enabled portions of the power reduction logic by adjusting transistor body bias.

40. A system for controlling power consumption, comprising:

a unit level device including one or more subunits;

a power control mechanism for selectively shutting down a portion of the unit level device;

at least one subunit device including a leakage current control device, comprising:

a circuit having one or more functions in a data

path where the functions are executed in a sequence, each of the functions having power reduction logic to selectively energize each respective function; and

a leakage control circuit, which interacts with the power reduction logic, so that the functions are energized or deenergized in a control sequence such the functions where the data is resident are energized and at least one of the other functions, is not energized.

41. The system as recited in claim 40, wherein the power reduction logic includes a sleep mode.

42. The system as recited in claim 40, wherein the power reduction logic is divided into individually enabled portions, each portion being enabled in accordance with the control sequence.

43. The system as recited in claim 40, wherein the power reduction logic is divided into individually enabled portions, each portion having a threshold voltage adjusted for transistors within each respective portion in accordance with the control sequence.

44. The system as recited in claim 43, wherein the threshold voltage for transistors is adjusted within each respective portion by controlling body biasing of the transistors.

45. The system as recited in claim 40, wherein the leakage control circuit selectively employs retentive and non-retentive means to reduce current leakage.

46. The system as recited in claim 45, wherein the retentive means includes body biasing of transistors.

47. The system as recited in claim 45, wherein the retentive means includes partial supply voltage and/or ground gating.

48. The device as recited in claim 45, wherein the nonretentive means includes supply voltage and/or ground gating.

49. The system as recited in claim 40, wherein the leakage control circuit controls power in the functions based on look-behind feedback from upstream functions in the data path.

50. The system as recited in claim 40, wherein the leakage control circuit controls power in the functions based on look-ahead feedback from downstream functions in the data path.

51. The system as recited in claim 40, wherein the leakage control circuit selectively controls power at the subunit level in conjunction with the power control mechanism to reduce current leakage and reduce power consumption.

52. The system as recited in claim 51, wherein individual components of the subunit device are controlled at a component level by the power reduction logic to selectively control power.

53. The system as recited in claim 40, wherein the power reduction logic is energized in accordance with a pulse wave.

54. The system as recited in claim 53, wherein the pulse wave is shorter than a clock cycle time.

55. The system as recited in claim 40, wherein the power reduction logic is energized in accordance with a

front edge of a pulse wave and at least partially deenergized in accordance with a back edge of the pulse wave.

56. The device as recited in claim 40, wherein the power reduction logic is divided into individually enabled portions such that only a subset of the portions are energized at a time.

57. The device as recited in claim 56, wherein a pulse wave controls the individually enabled portions of the power reduction logic by adjusting transistor body bias.